In the claims:

Please substitute the following full listing of claims for the claims as originally filed or most recently amended.

1. (Currently Amended) A method of forming a raised source/drain field effect transistor structure including a PFET and an NFET including the steps of:

forming gate structures including dual spacers at gate regions of a substrate;

etching said substrate adjacent said ~~a~~ gate region sufficient for silicidation of contacts in ~~a~~ said substrate;

~~forming a gate structure at said gate region;~~

growing boron doped amorphous silicon on NFET and PFET regions, adjacent said gate region, by selective epitaxy;

forming an abrupt source/drain junction for PFET boron extension electrode and NFET boron halo formation adjacent said gate region; and

selectively etching said dual spacers ~~in~~ at said source/drain junction.

2. (Currently Amended) The method of claim ~~2~~ 1, further comprising the steps of:

performing N-extension arsenic implantation and p-extension boron implantation; and

diffusing said arsenic and said boron such that said PFET extension electrode overlaps the gate region.

3. (Original) The method of claim 2, where the N-extension arsenic does not substantially overlap the gate region.

4. (Original) The method of claim 1, further comprising the step of performing selective amorphous growth to form the source/drain junction.

5. (Withdrawn) A CMOS structure comprising:

a gate region of a substrate sufficient for silicidation of contacts;

a gate structure at said gate region;

a PFET boron extension electrode and NFET boron halo, defining a source/drain junction, adjacent said gate region; and

permanent dual spacers in said source/drain junction.

6. (Withdrawn) The CMOS structure of claim 5, where the PFET extension overlaps the gate region.

7. (Withdrawn) The CMOS structure of claim 6, where the N-extension arsenic does not substantially overlap the gate region.